XEROX
BUSINESS SYSTEMS
Systems Development Department

To: Distribution

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Org: SDD/SD&T Workstation Design

Subject: **Workstation Structure**

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Our purpose, in this memo, is to describe the structure of the workstation processor. Several alternative designs have been evaluated. Workstation Design has adopted the approach that we feel is most advantageous in light of current technology and capability. Detail design is now underway. After 6-8 weeks of additional design, estimates of processor cost will be available.

The processor will be called Dandelion. The term Sumit (an acronym for synchronous multitasking) refers to a particular class of cpu designs. In the past there has been some confusion about the name of the processor.

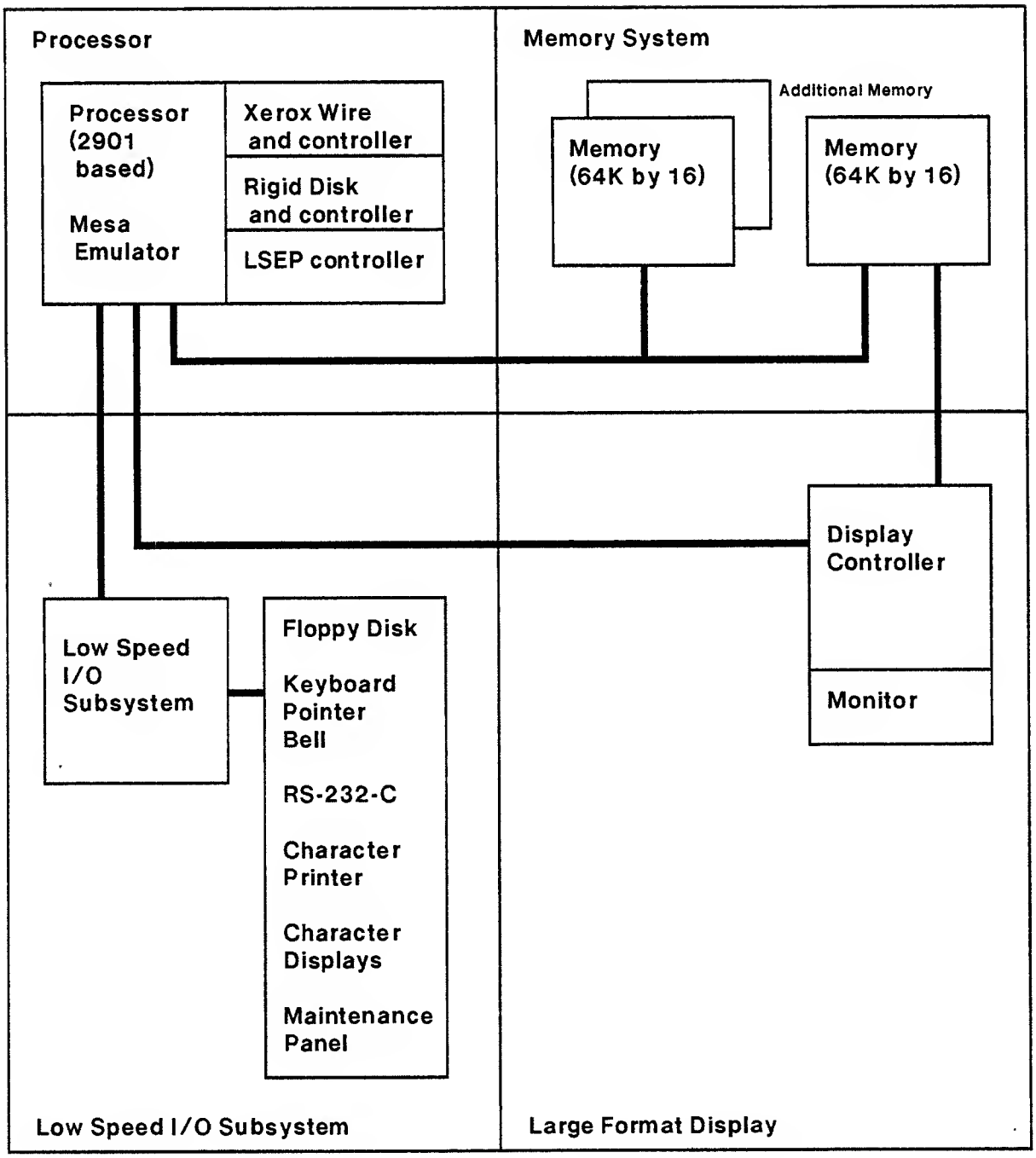
The figure, on page 2, shows a block diagram of the workstation processor.

Processor

The processor is designed to efficiently execute the mesa op codes defined in the *OIS Processor Principles of Operation Specification.*

The 2901 bipolar microprocessor slice is used to implement the heart of the cpu. These chips allow the flexibility and the performance necessary to handle the through-put requirements of mesa. The performance is expected to be about 500,000 mesa instructions per second. For comparison, the Alto executes abut 120,000 mesa instructions per second. Commercial microprocessors, such as Intel's 8086, were evaluated against the task of emulating the mesa language. However, these processors are from 5 to 50 times too slow to be acceptable.

The processor can also manage the controllers for 4 high performance peripherals in the workstation - large format display, Xerox Wire, rigid disk, and Low Speed Electronic Printer (LSEP). The Xerox Wire and rigid disk are controlled directly from the processor with a minimum of controller hardware. The Xerox Wire (which operates at 10M bits/second) uses 25% of the processor during packet transmission and reception. The rigid disk (7 Mbps for the SA4000 and 4 Mbps for the SA1000) uses less than 20%. Neither of these devices are active for more than a few percent of the execution of application programs. The savings in this approach over separate controllers is perhaps as much as two pwbs, $300 - to $600.



The Dandelion System

The large format display places a constant load of 40 to 50 million bits per second on the memory system. Special display hardware has been included in the design to insure that the processor in not overburdened. Processor management of this hardware, which includes cursor management, is estimated to take 3% of the processor.

The LSEP can be controlled using the processor and minimum controller hardware; however, because of the overall load on the system during printing, normal Star workstation functions must be suspended. The processor can be configured into a mini-server for the LSEP by excluding the large format display controller.

The processor also communicates with the low speed I/O subsystem to use a number of low speed devices. About 2% of the processor is consumed during peak transfer times.

Memory System

The memory structure is designed to take advantage of 64K memory chips now available (K=1024). The basic system includes a 64K by 16 bit memory bank that interfaces to the processor. This bank is synchronous with the processor, and cycles in approximately 400 ns. generating 40 M bits/second bandwidth for mesa and the high performance peripherals excluding the display. Additional 64K by 16 banks can be added to expand the total memory capacity.

A second memory bank, 64K by 16, is used to hold the bit map for the display. A separate display controller interfaces to this bank and transfers words to the display using the memory's "page mode" which allows a bandwidth of 60 to 80 M bits/second in this bank. The processor can also access this memory, using normal addressing, through a second port.

The memory system will include parity but probably not error correction. Initial reliability information indicates that error correction is not required. Implementing error correction is relatively costly.

The total memory capacity is planned to be 256K words.

Large Format Display

A separate display controller (about 30-60 chips) has been included in the design to do most of the work of maintaining an image on the crt. Control of this device and management of the cursor is done in the processor.

Low Speed I/O Subsystem

A commercial LSI microprocessor (probably an Intel 8085) will be used to control a variety of low speed devices are connected, namely:

1. floppy disk (IBM compatible or 850 compatible)
2. keyboard, pointer, and audio speaker (bell)
3. RS-232-C communication
4. connection of character displays (about 4 via limited RS 232)
5. connection of character printer (Mark IV via limited RS 232)

These devices will be connected to the system with off-the-shelf LSI components. The microprocessor will also control system booting, control store management, and diagnostics.

Reference Documents

[1] Belleville, R. et. al., *Workstation Processor Summary*, Systems Development Department (Memo w/ attachments), February 19, 1979. Filed on [IRIS] <Workstatiion> Notes> WS-Summary.press (62 pages)

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